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## Description

# DETECTION OF HARDMASK REMOVAL USING A SELECTIVE ETCH

### BACKGROUND OF INVENTION

#### [0001] Technical Field

[0002] The present invention relates generally to interconnect semiconductor structures, and more particularly, to a method of detecting devices lacking at least a portion of a protective hardmask covering an underlying material.

#### [0003] Related Art

#### [0004]

A hardmask can be deposited over a dielectric layer during the formation of damascene structures. The hardmask acts as an etch stop layer and/or a chemical-mechanical polish (CMP) stop layer during the formation of conductive features within the dielectric layer. The hardmask also acts as a protective barrier preventing ambient moisture from diffusing into the dielectric layer. Moisture that diffuses into the dielectric layer can eventually attack the conductive features within the dielectric layer and lead to catastrophic device failure. Clearly, it is undesirable to have regions of the dielectric layer that do not have the

protective hardmask thereover.

[0005] Unfortunately, portions of the hardmask can be inadvertently removed during the chemical-mechanical polishing (CMP) of the conductive features within the dielectric layer. This is particularly problematic in regions of high metal density. Regions are considered high metal density regions when the ratio of the conductive features to the spaces between the conductive features is greater than 50%. For example, a grouping of conductive wires having a width of 1.8 microns spaced about 0.2 microns apart would be characterized as having 90% metal density. This type of region would be especially susceptible to hardmask removal. The removal of the hardmask occurs because the CMP polishes through the conductive material, e.g., copper, much faster than the hardmask. Since the conductive features are so close together the small islands of hardmask extending above the plane of the conductive features are often removed during the CMP polish.

[0006] The problem arises in detecting those devices having regions that are lacking the protective hardmask before the device is implemented, or shipped to the end user. Therefore, there is a need in the industry for a method of detecting devices having regions lacking a protective hardmask.

## SUMMARY OF INVENTION

[0007] The present invention provides a method that solves the above problems associated with the formation of an interconnection structure.

[0008] A first aspect of the invention provides a method of detecting an interconnection structure having a region within a first wiring level wherein a second layer is not covering a first layer, comprising: providing the first layer having the second layer on a surface of the first layer; and creating a recess in the first layer in the region where the second layer is not covering the first layer.

[0009] A second aspect of the invention provides a structure comprising: a first wiring level of the structure comprising: a first layer covering a surface of the structure; a second layer substantially covering a surface of the first layer; and a recess formed in a region of the structure where the second layer does not cover the first layer; and a second wiring level of the structure comprising: a third layer having a replicated recess in the third layer in the region of the structure where the second layer does not cover the first layer.

[0010] A third aspect of the invention provides a method of forming an interconnection structure, comprising: using recessed topography formed within a first layer of the structure to indicate the absence of a hardmask covering the first layer.

[0011] The foregoing and other features and advantages of the invention will be apparent from the following more particular description of the embodiments of the invention.

## BRIEF DESCRIPTION OF DRAWINGS

[0012]

The embodiments of this invention will be described in detail, with

reference to the following figures, wherein like designations denote like elements, and wherein:

- [0013] Fig. 1 depicts a first dielectric layer and a first hardmask of an interconnection structure;
- [0014] Fig. 2 depicts the formation of trenches within the first dielectric layer and first hardmask of the structure of Fig. 1;
- [0015] Fig. 3 depicts deposition of a conductive material within the trenches of Fig. 2 forming the dual damascene conductive features within a first wiring level;
- [0016] Fig. 4 depicts the first wiring level of the dual damascene structure having a region of the first dielectric layer that is missing the first hardmask;
- [0017] Fig. 5 depicts the structure of Fig. 4 having a step formed in the region of the first dielectric layer missing the first hardmask;
- [0018] Fig. 6 depicts a second wiring level of the structure of Figs. 4 and 5 wherein the step in the first wiring level is replicated in the second wiring level;
- [0019] Fig. 7 depicts the structure of Fig. 6 following the formation of trenches within the second dielectric layer and second hardmask of the second wiring level;
- [0020] Fig. 8 depicts deposition of a conductive material within the trenches of Fig. 7 forming the dual damascene conductive features in the second

wiring level;

[0021] Fig. 9A depicts a photograph of a structure having a shorted region and a non-shorted region;

[0022] Fig. 9B depicts a drawing illustrating proper formation of a structure;

[0023] Fig. 10A depicts a structure in accordance with a second embodiment of the present invention before etching; and

[0024] Fig. 10B depicts a structure in accordance with a second embodiment of the present invention after etching.

## DETAILED DESCRIPTION

[0025] Although certain embodiments of the present invention will be shown and described in detail, it should be understood that various changes and modifications might be made without departing from the scope of the appended claims. The scope of the present invention will in no way be limited to the number of constituting components, the materials thereof, the shapes thereof, the relative arrangement thereof, etc. Although the drawings are intended to illustrate the present invention, the drawings are not necessarily drawn to scale.

[0026] The present invention is applicable to the formation of semiconductor interconnect structures, i.e., those structures containing high electrical conductivity metals or alloys, such as copper, aluminum, silver, etc. The formation of a dual damascene structure is described herein for the purposes of illustration only. The disclosure is equally applicable to the formation of a single damascene structure, as well as numerous other

interconnect structures.

[0027] Fig. 1 shows a first metal wiring level 12 of an interconnection structure 10. The first metal wiring level 12 includes a first dielectric layer 14, and a first hardmask 16 deposited over a surface 18 of the first dielectric layer 14. The first dielectric layer 14 and the first hardmask 16 are formed using techniques well known to those skilled in the art. The first dielectric layer 14 may comprise a dielectric material that etches selectively to the first hardmask 16, and may have an effective dielectric constant within the range of 1-4, optimally 2-3. For example, the first dielectric layer 14 may comprises a SiLK<sup>TM</sup> (Dow Chemical Company) semiconductor dielectric resin, or any polymer dielectric, such as, Teflon, bezocyclobutane-BCB, parylene-N, parylene-F, SiCOH, porous SiO<sub>2</sub>, silica aerogels, and Flare<sup>TM</sup> (Honeywell), etc. The first hardmask 16 may comprise one or more layers of inorganic materials, such as SiN<sub>x</sub>, SiO<sub>x</sub>N<sub>y</sub>, SiC<sub>x</sub>, SiO<sub>x</sub>C<sub>y</sub>, SiC<sub>x</sub>N<sub>y</sub>, SiO<sub>2</sub>, and SiC<sub>x</sub>O<sub>y</sub>H<sub>z</sub>, or other similarly used materials having a significantly lower etch rate than the first dielectric layer 14. It should be noted that the first hardmask 16 is shown having only one layer for ease of illustration, but may comprise multiple layers. The first hardmask 16 acts as a protective barrier preventing moisture from diffusing into the first dielectric layer 14.

[0028]

The first hardmask 16 also prevents the first dielectric layer 14 from being damaged during CMP, reactive ion etch (RIE), photoresist strip processes, and other similar processes performed during the formation

of the structure 10. As mentioned in the Background, moisture that diffuses into the first dielectric layer 14 can eventually attack the conductive features within the first dielectric layer 14 and lead to catastrophic device failure. The first hardmask 16 also acts as an etch stop layer during the formation of conductive features within the first dielectric layer 14.

[0029] As illustrated in Fig. 2, a first trench 20a, 20b is formed within the first dielectric layer 14 in the location of a first and a second conductive feature, respectively, (see Fig. 3). A second trench 22a, 22b, 22c is formed within the first dielectric layer 14 in the location of the first, second and third conductive features, respectively, (see Fig. 3). As illustrated, the first and second trenches 20a-b, 22a-c have different cross-sections. The first and second trenches 20a-b, 22a-c are formed in accordance with processes known in the art. As illustrated in Fig. 3, a liner 24, that conformally coats the inner walls of the first and second trenches 20a-b, 22a-c, is deposited within the first and second trenches 20a-b, 22a-c forming via and wire trenches, respectively. The liner 24 may comprise a refractory metal, such as tantalum-based materials, tungsten-based materials, titanium-based materials, or other similar materials, or other refractory metals, and may be deposited using known deposition techniques. The liner 24 prevents the conductive material that will be deposited within the first and second trenches 20a-b, 22a-c from diffusing into the first dielectric layer 14.

[0030]

As illustrated in Fig. 3, the first and second trenches 20a-b, 22a-c are

then filled with a conductive material 26, such as copper, gold, platinum, silver, etc. The conductive material 26 may be deposited using known deposition techniques, such as plasma vapor deposition (PVD), chemical vapor deposition (CVD), or other techniques.

Following deposition of the conductive material 26, a chemical-mechanical polish (CMP), or other similar polishing technique, may be used to remove excess conductive material 26 extending beyond, and on top of, a surface 29 of the hardmask 16, thereby forming a first conductive feature 31, a second conductive feature 33 and a third conductive feature 35. In this example, the first trench 20 (see Fig. 2) forms a conductive via 28 of the conductive features 31, 33 and the second trench 22 (see Fig. 2) forms a conductive line or wire 30 of the conductive features 31, 33, 35.

### [0031]

Prior to the formation of a subsequent or second metal wiring level 112 (see Figs. 6-8), a capping or barrier layer 36 is deposited over the exposed surface 29 of the first metal wiring level 12 (refer to Fig. 6).

The capping layer 36 prevents the copper 26 within the conductive features 31, 33, 35 from diffusing into the second dielectric layer 114 within the second wiring level 112 (see Figs. 6-8) during processing.

The capping layer 36 can also be used as a RIE stop layer for subsequent via formation. As is known in the art, however, there are often problems adhering an inorganic capping layer 36 to the copper 26 within the conductive features 31, 33, 35. Therefore, prior to the deposition of the capping layer 36 the exposed copper 26 within the

conductive features 31, 33, 35 is subjected to a reducing plasma preclean process.

[0032] Conditions and reducing plasmas similar to those described in US 6,261,951 B1 and US 6,255,217 B1 may be used, and are incorporated herein by reference. For example, reducing plasmas such as H<sub>2</sub>, N<sub>2</sub>, NH<sub>3</sub>

[0033] and noble gases such as nitrogen, helium, etc., may be used in the present invention. The reducing plasma preclean process may be performed in a conventional plasma deposition apparatus that is capable of generating plasma gas.

[0034] The reducing plasma preclean process not only causes the capping layer 36 to adhere to the copper 26 within the conductive features 31, 33, 35, but the conditions of the process can be manipulated in order to detect devices that have regions 34 of the first hardmask 16 missing from the surface 18 of the first dielectric layer 14, or are of an insufficient thickness to protect the first dielectric layer 14, e.g., a thickness less than 50 nm. As mentioned in the Background, regions 34 of the first dielectric layer 14 where the first hardmask 16 is missing are susceptible to the diffusion of water into the first dielectric layer 14 (refer to Fig. 4). The water may then attack the copper 26 within the conductive features 31, 33, 35, which in turn can lead to catastrophic device failure. Therefore, it is undesirable to have regions 34 wherein the first hardmask 16 is missing from, or not sufficiently covering, the first dielectric layer 14. In accordance with the present invention, the

reducing plasma preclean process is used to intentionally damage any device 110 wherein the first hardmask 16 is missing from, or not covering, the surface 18 of the first dielectric layer 14.

[0035] In particular, the plasma used in the reducing plasma preclean process selectively etches the first dielectric layer 14 with a selectivity preferably greater than 10:1 which leaves the first hardmask 16 nearly unetched. In an optimal embodiment the selectivity of the reducing plasma preclean process would be infinite.

[0036] Figs. 4 and 5 illustrate the selectivity of the reducing plasma preclean process. Fig. 4 shows a structure 110 before the reducing plasma preclean process is performed. The structure 110 has a first region 34 where the first hardmask 16 is not covering the surface 18 of the first dielectric layer 14, and a second region 37, a third region 39 and a fourth region 41 where the first hardmask 16 is covering the first dielectric layer 14. The first hardmask 16 may have been inadvertently removed in region 34 during the CMP process, or other similar process, used to planarize the conductive features 31, 33, 35. Fig. 5 shows the structure 110 after the reducing plasma preclean process has been performed. At least a portion of the first dielectric layer 14 has been removed in region 34, to a depth D, by the reducing plasma preclean process, creating a recessed topography or a step 32 in the region 34 where the first hardmask 16 was not covering the first dielectric layer 14. In contrast, the first dielectric layer 14 is not etched in regions 37, 39, 41 where the first hardmask 16 covers the first dielectric layer 14.

As clearly illustrated, the region 34 of the first dielectric layer 14 that does not have the first hardmask 16 thereover will be etched during the reducing plasma preclean process, while the regions 37, 39, 41 of the first dielectric layer 14 that do have the first hardmask 16 thereover will not be etched.

[0037] It should be noted that only one region 34 is shown lacking the first hardmask 16, consequently, only one step 32 is created in the first dielectric layer 14. This is intended for simplicity of illustration only, and is in no way intended to limit the scope of the invention.

[0038] As illustrated in Fig. 6, the optional capping layer 36 is then deposited over the surface 29 of the structure 110 following the reducing plasma preclean process has been performed. Because the reducing plasma preclean process etches the surface of the copper 26 within the conductive features 31, 33, 35, the capping layer 36 adheres properly to the surface 29 of the structure 110. The capping layer 36 may comprise an inorganic material, such as SiC, SiN, or other similar materials. The capping layer 36 may be deposited using conventional vapor deposition techniques, such as chemical vapor deposition, low pressure chemical vapor deposition, high pressure chemical vapor deposition, high density plasma chemical vapor deposition (HDPCVD), plasma enhanced chemical vapor deposition (PECVD), and other similar vapor deposition techniques.

[0039] Thereafter, the layers of a second wiring level 112 are deposited. In particular, a second dielectric layer 114 is deposited over the capping

layer 36, and a second hardmask 116 is deposited over the second dielectric layer 114. Because the capping layer 36, second dielectric layer 114 and second hardmask 116 are conformal, or partially conformal, the step 32 created in the first wiring level 12, due to the missing hardmask 16, is replicated as a second recessed topography or replicated recess or step 132 in second wiring level 112.

[0040]

As illustrated in Fig. 7, a first trench 120a, 120b is formed within the second dielectric layer 114 in the location where a first and a second conductive feature, respectively, of the second wiring level 112 are supposed to be formed. A second trench 122a, 122b, 122c is formed within the second dielectric layer 114 in the location where the first, second and third conductive features, respectively, of the second wiring level 112 are supposed to be formed. The first and second trenches 120a-b, 122a-c are patterned and etched in accordance with processes known in the art, and are normally similar to the conductive features formed in the first wiring level 12 (see Fig. 3). The first and second trenches 120a-b, 122a-c may also include an optional liner 124 conformally coating the inner walls of the first and second trenches 120a-b, 122a-c. As with the liner 24 of the first wiring level 12, the liner 124 of the second wiring level 112 may comprise a refractory metal, such as tantalum-based materials, tungsten-based materials, titanium-based materials, or other similar materials, and may be deposited using known deposition techniques. The liner 24 prevents the conductive material that will be deposited within the first and second trenches

120a-b, 122a-c from diffusing into the second dielectric layer 114.

[0041] As Fig. 7 illustrates, the trenches 122a and 120b that are adjacent the replicated step 132 (see Fig. 6) in region 34 are not formed properly. Specifically, the second trench 122a of the first conductive feature 131 (Fig. 8) and the first trench 120b of the second conductive feature 133 (Fig. 8) cut into the replicated step 132. As a result, the boundaries of the second trench 122a of the first conductive feature 131 and the first trench 120b of the second conductive feature 133 do not exist. Rather, the second trench 122a of the first conductive feature 131 and the first trench 120b of the second conductive feature 133 blend together with the replicated step 132 (Fig. 6). It should be noted that the dotted lines are inserted only for clarity to show where the replicated step 132 is located with respect to the trenches 122a, 120b, no boundaries actually exist. In contrast, the trenches 120, 122 adjacent to regions 37, 39, 41 of the structure 110, where the first hardmask 16 covers the first dielectric layer 14, are formed properly. Specifically, going from left to right, the first trench 120a adjacent region 41, the second trench 122b adjacent region 37 and the second trench 122c adjacent region 39 are formed properly.

[0042]

It should be noted that the replicated step 132 in the second wiring level 112 replicates to a depth D1, and the second trench 122a is formed to a depth d. In this example, the depth D1 of the replicated step 132 is less than the depth d of the second trench 122a. The replicated step 132, however, may be formed to a depth D1 greater

than, or equal to, the depth d of the second trench 122a.

[0043] As illustrated in Fig. 8, the replicated step 132 (Fig. 7) and the first and second trenches 120a-b, 122a-c are filled with a liner 124 and a conductive material 126, as described above. Following deposition of the conductive material 126, a chemical-mechanical polish (CMP), or other similar polishing technique, may be used to remove excess liner 124 and conductive material 126 extending beyond, and on, a surface 129 of the second hardmask 116.

[0044] A third conductive feature 135 in the second wiring level 112 is formed properly, similar to the third conductive feature 35 of the first wiring level 12. A first 131 and a second 133 conductive feature of the second wiring level 112, however, are not formed properly in a manner similar to the first 31 and second 33 conductive features of the first wiring level 12. Rather, the replicated step 132 in the second wiring level 112 (see Fig. 7) fills with conductive material 126 producing an electrically shorted region 152 between what was supposed to be the first and second conductive features 131, 133. Due to the electrical short the device will not function properly. Non-functioning devices are removed from a batch of devices, thereby protecting the manufacturer from inadvertently implementing a defective device, or sending a defective device to an end user.

[0045] Fig. 9A is a photograph showing a top view of a structure 500 similar to structure 110 that had a recess formed within a first dielectric layer thereby creating an electrical short. In particular, Fig. 9A shows a

plurality of wires 501-505 and a plurality of vias 506-509. Wires 501, 502 and vias 506, 507 are electrically shorted together because region 510 between wires 501, 502 and vias 506, 507 was lacking sufficient first hardmask 16 to prevent etching of the first dielectric layer 14 during the reducing plasma preclean process (see Figs. 1-8). In contrast, the wires 503-505 and vias 508, 509 are not electrically shorted together because there was sufficient first hardmask 16 surrounding the wires 503-505 and vias 508, 509 to prevent etching of the first dielectric layer 14 during the reducing plasma preclean process. Fig. 9B is a drawing of a similar structure 600 that illustrates a properly formed structure. Specifically, wires 601, 602 and vias 606, 607 are not shorted together in region 610 because there was a sufficient amount of first hardmask 16 covering the first dielectric layer 14 in region 610 to prevent the reducing plasma preclean process from etching the first dielectric layer 14 in region 610.

[0046] The degree to which the first dielectric layer 14 is etched in the regions 34 where the hardmask 16 is not covering the first dielectric layer 14 depends upon the conditions of the reducing plasma preclean process. Steps 32 having a sufficient depth D, in this example a depth D of approximately 100 nm or greater, will produce shorts within the second metal wiring level 112. Obviously, the deeper the step 32 formed by the reducing plasma preclean process, and the faster the step 32 is formed, the more easily the defective device will be shorted and be discovered.

[0047] The outcome of the reducing plasma preclean process varies depending upon the conditions selected from a group of preclean conditions. The group of preclean conditions that may be varied during the reducing plasma preclean process include the etching or plasma material used to preclean the surface of the conductive features 31, 33, 35, the temperature at which the process is performed (room temperature to 500 Å°C), the time or duration of the process (10-60 seconds), the pressure at which the process is performed and the rf power. Varying at least one of the conditions in the group of preclean conditions will alter the depth D of the step 32 in the first dielectric layer 14.

[0048] Therefore, the preclean conditions can be intentionally manipulated to produce the desired step 32 depth D within the first dielectric layer 14. Several examples follow that illustrate the effect of altering different preclean conditions of the reducing plasma preclean process on the creation of steps 32 within the first dielectric layer 14. It should be noted that these are not intended to encompass all the possible reducing plasma preclean process conditions and results.

[0049] Example 1:

[0050] The temperature at which the reducing plasma preclean process is performed can alter the depth D to which the step 32 is created within the first dielectric layer 14. As mentioned above, the temperature may range from room temperature to approximately 500 Å°C.

[0051] An H<sub>2</sub> reducing plasma preclean process, performed at approximately 5 mTorr and 4500 W rf power, will etch a SiLK dielectric layer 14 of a 200 mm wafer in areas where a first hardmask 16 is missing to a depth D at a rate of approximately 1.0 microns per minute at 100 °C. In contrast, under the same conditions the H<sub>2</sub> reducing plasma preclean process will etch to a depth D at a rate of approximately 2.0 microns per minute at 400 °C. Clearly, in this example it is advantageous to perform the reducing plasma preclean process at a higher temperature because it produces deeper steps 32 within the first dielectric layer 14 for a given etch time. In turn, the device is more likely to produce shorts within the second or subsequent wiring levels, and is therefore easier to detect as a failed device.

[0052] Example 2:

[0053] The use of different plasma materials may also alter the depth D to which the steps 32 are created within the first dielectric layer 14. As mentioned above, reducing plasmas such as H<sub>2</sub>, N<sub>2</sub>, NH<sub>3</sub> and noble gases such as nitrogen, helium, etc., may be used in the present invention.

[0054] During a ~30 second plasma heat-up step a HDPVD process etches a SiLK dielectric layer 14 to a depth of approximately 1000 nm. In contrast, during about a ~30 second plasma heat-up step a nitrogen plasma etches a SiLK dielectric layer 14 to a depth of approximately 800 nm.

[0055] Example 3:

[0056] A PECVD process, using NH<sub>3</sub> plasma, a parallel plate reactor, a heated wafer chuck, performed at 5 Torr and an rf power of 500 W for 20 seconds will etch 200nm of SiLK dielectric within a 200 mm wafer.

[0057] The above has described and illustrated the present invention in terms of a recess 32 that is etched to a depth D that is less than the depth 100 of the first dielectric layer 14 (see Fig. 5). Figs. 10A and 10B illustrate an alternative structure 210 wherein the depth D of the recess 232 is approximately equal to the depth 400 of a first dielectric layer 214. As a result, conductive features 231, 233 have no support on at least one side of the conductive feature 231, 233 and fall over onto adjacent conductive features 235, 237, respectively. This results in catastrophic device failure in this, as well as the second wiring level (not shown) constructed thereon.

[0058] As mentioned above, the structure is susceptible to recess formation in regions where the first hardmask 16 is completely missing from the surface of the first dielectric layer 14. Although also mentioned above, it should be emphasized that regions where the first hardmask 16 covers the first dielectric layer 14 but has a thickness much less than 50nm may also become etched during the reducing plasma preclean process because the reducing plasma preclean process does not have infinite selectivity to first hardmask 16. As a result, recesses in first dielectric layer 14 will form in these regions as well.

[0059] While this invention has been described in conjunction with the specific embodiments outlined above, it is evident that many alternatives, modifications and variations will be apparent to those skilled in the art. Accordingly, the embodiments of the invention as set forth above are intended to be illustrative, not limiting. Various changes may be made without departing from the spirit and scope of the invention as defined in the following claims.